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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,382	10/01/2003	Katsuhiko Hieda	04329.3151	4438

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EXAMINER	
TRAN, BINH X	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,382	HIEDA ET AL.	
	Examiner	Art Unit	
	Binh X. Tran	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-23* is/are allowed.

6)☒ Claim(s) *1-8 and 10-14* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-01-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. Figure 1A-1F, 2A-2C, 3A-3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyanagi (US 6,191,002) in view of Goo et al. (US 6,489,252).

Respect to claim 1, Koyanagi disclose a method of manufacturing a semiconductor device comprising the steps of:

forming an element isolation trench (3) in a semiconductor substrate (1) by using a mask member (6) (Fig 4B-4C);

forming a first film (7) on the substrate by a coating method to fill the element isolation trench with the first film (Fig 4D);

evaporating a solvent contained in the first film to convert the first film into a second film (step S1, col. 8 lines 25-30);

subjecting the second film buried in the element isolation trench (3) to burning oxidation treatment in an atmosphere containing water vapor (col. 8 lines 31-54).

Koyanagi fails to disclose the step of removing the second film which is deposited on the mask member by CMP, thereby permitting a surface of the mask

member to expose while selectively leaving behind part of the second film which is buried in the element isolation. However, Koyanagi clearly discloses the step of CMP the oxide film (4) deposited on the mask member, thereby permitting a surface of the mask member to expose while selectively leaving behind part of the oxide layer (4) which is buried in the element trench isolation (Fig 4E-4F, col. 8 lines 60-67). In a semiconductor method, Goo teaches to CMP the polysilazane layer (second layer after evaporating the solvent via curing) in the first film (col. 2 lines 43-65). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Koyanagi in view of Goo by CMP the second film because this technique is capable of polishing a polysilazane layer to form a smooth surface without forming additional cap layer.

Respect to claim 5 and independent claim 10, Koyanagi discloses the step of coating a solution of silazane perhydrogenated polymer on a surface of the semiconductor substrate by a coating method to film the element isolation trench (3) (col. 8 lines 1-20). Koyanagi and Goo teaches to heat-treat the silazane perhydrogenated polymer to evaporate the solvent, thereby converting the coated film into a polysilazane film (Koyanagi's col. 8 lines 26-30; Goo's col. 2 lines 51-67). The limitation regarding the burning oxidation treatment has been discussed above.

Respect to claims 2 and 12, Koyanagi discloses the burning oxidation is performed at 400 °C in an atmosphere containing water (col. 8 lines 31-37).

Respect to claims 3 and 13, Koyanagi discloses the step burning oxidation includes a low temperature heat treatment (col. 8 lines 31-37). Koyanagi fails to

disclose the high temperature heat treatment step in the burning oxidation process. Goo teaches both low temperature heat treatment (i.e. hard bake at 400-450 °C) and high temperature heat treatment (700-900 °C) under oxidation atmosphere including water vapor (col. 5 line 57 to col. 6 lines 30). It would have been obvious to one having ordinary skill in the art, at the time of invention, to modify Koyanagi in view of Goo by including high temperature treatment because this will increase the curing effect.

Respect to claim 4, Koyanagi disclose the width of the trench is 0.1 μm and aspect ratio equals to 5 (col. 8 lines 14-15). Aspect ratio is defined as the ratio of the depth divided by the width (See prior art made of record). Base on this definition, the depth of the trench equal to 0.5 μm (depth = aspect ratio * width = 5 * 0.1 = 0.5 μm = 500 nm; within applicant's range).

Respect to claim 6, Goo discloses the heat treatment of the second film is performed prior to removal of part of the second film by using CMP process (col. 8 lines 53-55). Respect to claim 7, Koyanagi discloses the temperature of heat treatment is at 400 °C in an atmosphere containing water vapor (col. 8 lines 31-35, within applicant's range). Goo also discloses the temperature of 400-450 °C in an atmosphere containing water vapor (col. 5 lines 57-58; col. 6 lines 6-8).

Respect to claims 8 and 14, Koyanagi discloses subjecting the second film to a densification at the temperature of 900 °C subsequent to the burning oxidation treatment of the second film (col. 8 lines 54-59, Fig 3 step S3; within applicant's temperature range). Respect to claim 11, Koyanagi discloses the step of heating treating the silicon oxide film (4) to enhance a density of the silicon oxide film (col. 8

lines 54-59); and removing the mask member (5 and/or 6) depositing on the substrate subsequent to forming the silicon oxide film (4) (Fig 6D-6E).

Allowable Subject Matter

6. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 15-23 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: The cited prior arts fail to suggest or disclose either one of the following step in conjunction with all other limitation in the claims: the mask member is removed form the semiconductor substrate to permit sidewalls of the second film to expose prior to the densification treatment; or peeling the base film from the dielectric film to obtain the semiconductor substrate having said step portion buried in the dielectric film, thus forming a dielectric film having a flat surface. The closes prior art (Koyanagi) teaches to remove the mask member after the densification treatment.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin et al (US 2004/0043581) define aspect ratio equals depth/width (paragraph 0043).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh X. Tran whose telephone number is (571) 272-

1469. The examiner can normally be reached on Monday-Thursday and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tran

Binh X. Tran